Implementation of Decimating Filter in 5G System for Area and Power Optimization Using FPGA

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Abstract: One of the key components in the baseband section of a 5G system is the filter decimator unit. This unit helps to remove the excess bandwidth and reduce the sampling frequency of the given signal. The existing decimator filter works at higher frequency. As the power increases the frequency increases and vice-versa, this filter often consumes more power. Also, the area consumption is high. The main idea of the project is to modify the architecture of the decimator filter such that, it will consume lower area and power. The final architecture will be realized for Spartan 3e FPGA.

Keywords: 5G systems; Baseband section; Sampling frequency; Spartan 3e FPGA; Area; Power

I. INTRODUCTION

Communication is a process of propagation of information by different mediums. It could also be addressed as a universal phenomenon. The information is transmitted from the sender to the receiver through the communication channel. Mobile communication is widely used for audio signals, they are wireless and are not restricted to a particular location.

There are 5 generations in mobile communication 1G, 2G, 3G, 4G, and 5G.

1G (1st Generation): The first calls worked only on analog signals. It used Frequency-Division Duplexing scheme with speed of 24kbps and bandwidth of 25Mhz.

2G (2nd Generation): This generation was working on digital systems and supported voice and SMS. It supports four sectors of mobile communication industry namely digital cellular, mobile data, personal communications service, and Wireless-LAN, and has a speed of 64 kbps.

Using the concept of GPRS, 2.5G was introduced which was 2G's successor. 2.72G was introduced which is also called as EDGE and was providing faster services.

3G (3rd Generation): This generation was an upgrade, which had fasted speeds, better internet system, better system capacity and worked on UMTS and WCMA models, and has a speed of 2 Mbps.

4G (4th Generation): This generation is based on IP protocols; with the introduction of LTE and Vo-LTE the performance is boosted. It also supports HD quality streaming in multimedia service at low transmission cost and has speeds of 100 Mbps.

5G (5th-Generation): 5G refers to the fifth-generation of mobile technology for broadband networks. Wireless services will be enhanced with increased speed, reduced latency, and flexibility. The speed is 30 times faster than 4G.

Properties of 5G Technology:

- In addition to high resolution and a large bandwidth, 5G technology offers a bi-directional connection
- 5G technology also allows subscribers to monitor their own activity.
- Nearly 65000 connections can be supported with 5G technology, allowing for large data streams at gigabit speeds.
- The 5G technology can support virtual private network (VPN).

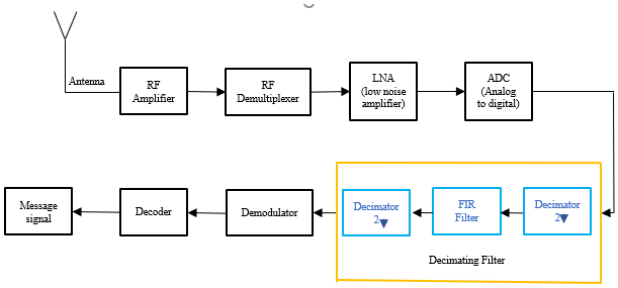

Fig 1. Block diagram of 5G receiver system

To reduce area and power and to enhance high speed data rates, wideband frequency selection is necessary because of advancements in the semiconductor industry and 5G communications. All of these requirements can be met with FIR filter decimators because of their non-feedback nature, linear phase, and stability. When compared to IIR filters, FIR filters have a lower degree of stability because they do not have a feedback mechanism. FIR filters are widely used because of their linear phase response. By choosing the FIR coefficients correctly, you can achieve linear phase. Linear phase requires symmetrical coefficients around a center coefficient.

II. LITERATURE SURVEY

In [1]. a novel multi-objective optimal strategy is developed to meet the requirements of commercial ADC specifications by using the multistage decimation filter. An equiripple FIR filter is applied at different stages during this filtering process to compensate overall performance. This helps in reduction of cost and minimising the group delay.

According to [5], considering CIC decimator, the two modifications has been done. Initially, Integrator comb pair is replaced by Integrated and Dump block that performs same operation. This replaced block is called as CIC-ID. There is also a time-multiplexed comb that replaces the remaining comb filters and the resulting data path is referred to as CIC-ID-TMUX. Due to this replacement the area consumption is optimized.

This paper [7] presents decimator with flat passband using sample rate conversion filter. Linear programming optimization (LPO) is proposed to reduce computational costs while improving the magnitude response of filters. The architecture consists of a CIC compensator and compensated SCIC. It reduces hardware complexity i.e., area consumption.

In [9], the motive of this paper is to protect transmission lines from high sampling rates using travelling wave protection system. For the protection the decimator filter circuit is designed and provided with high sampling rates, these high samples will be decimated and filtered, using Remez exchange algorithm group delay will be controlled and by sparse filter design and multistage approach algorithm the computational cost will be reduced.

III. METHODOLOGY

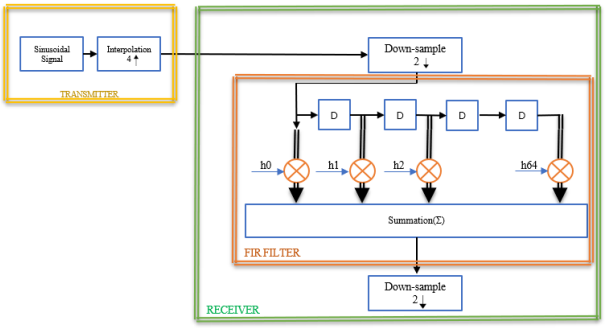

Fig 2. Block diagram of Decimating-filter

The decimator-filter lies between the analog to digital converter and the demodulator. It comprises of mainly two blocks:

- FIR filter
- Decimator

A. *FIR Filter*

Lowpass FIR filters in which the cut-off frequency can be tuned at run-time can be implemented using DSP Variable Bandwidth FIR Filter. Although these filters don't provide the same level of control over the response characteristic, they can be tuned to produce a dynamic response.

B. *Decimator*

Decimation is a method of reducing the sampling rate. It is also called as down sampling which some of the samples are discarded. Decimation is done when a passed signal is having a low sampling frequency and is sent to the neighboring system which requires a low sampling rate and also to reduce the processing and functional cost.

The calculation and memory required for DSP system increases with high sampling rate. Thus, use lower sampling rate for cheaper implementation. Decimation is defined as the ratio between input and output. It is denoted by "M".

Applications of decimator-filter:

- Decimation filters help us remove the excess bandwidth.
- It reduces the sampling frequency of the signal.
- It also helps us to reduce the computational resources required for processing and storing the signal.

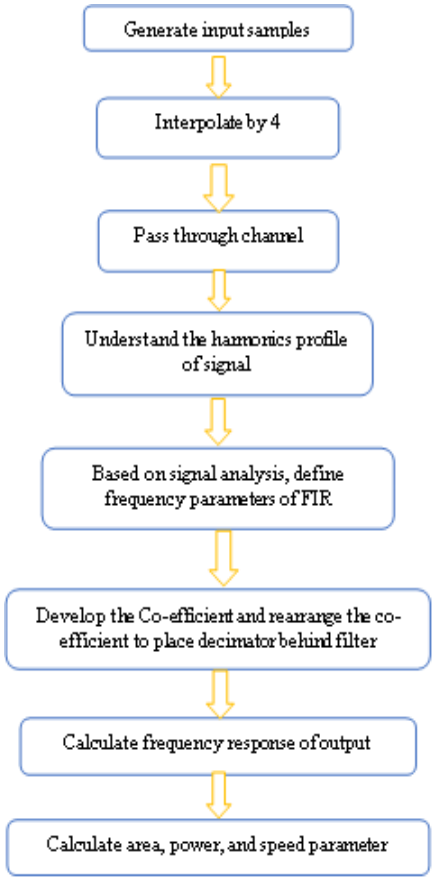

Fig 3. Implementation

IV. RESULTS

Properties	**Existing**	**Proposed**
Area	69%	31%
Time	70.321ns	38.801ns
Power	0.00115W	0.00074W

Table 1. Comparison table

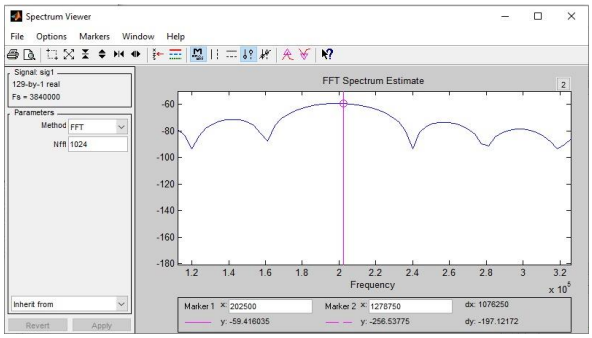

Fig 4. Frequency response of the output

The Verilog codes written are downloaded on FPGA. The frequency response of the output obtained from the FPGA is calculated to verify whether the original message signal is obtained. This is performed by calculating FFT of the output signal obtained from FPGA.

V. CONCLUSION

We can conclude that the area, power and speed has been enhanced when decimation by 2 is done in 2 steps rather than a single decimation by 4. This reduces the consumption of power at the receiver thus, increases the battery life of wireless devices. The area and speed optimizations help in better architecture and design of the device.

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