Designing of 4G Baseband Receiver Filter – Decimator Module

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Abstract: Filter decimator model is the most integral part of baseband wireless receivers. At the receiver an Intermediate Frequency (IF) signal is converted to Baseband signal. This conversion is done in three stages - mixing, decimation and filtering. Because of this reason, the architecture of the filter and decimator consumes more area and power. In this paper, an improvised architecture of filter and decimator has been presented. Modelsim software was used for implementation of the idea. The results suggest that the proposed model of the 4G receiver consumes less power and area than the existing method.

Keywords: 4G; RRC Filter; Decimator; NCO; Folded FIR filter

I. INTRODUCTION

Wireless communication is a scheme of data transfer between two or more points which are not connected over physical medium. Radio communication is commonly used for wireless technology, as it is very fast. It is used in mobile and portable applications like two-way radios, cellular telephones, personal digital assistants (PDAs), and wireless networking. Types of wireless communications are Radio communication, Microwave communication (antennas, or short-range communication), Light visible and infrared (IR) communication (IR devices such as remote controls or via Infrared Data Association), Sonic (ultrasonic short range communication), Electromagnetic induction short range communication, Wi-Fi technology.

Wireless receivers comprised of infrared frequency, radio frequency and baseband receivers. IR communication is used for short distance applications. We can reuse the frequency in IR communication; it achieves high bit rate, low signal processing complexity and low cost. But the challenges in IR communication are low SNR. RF receivers perform amplification, down-conversion and filtering. Baseband transmission is a direct digital data transmission without any modulation scheme. Baseband receiver consists of receiving filter (matched filter and correlator), equalizing filter, sampler and detector.

4G baseband receiver is similar to its other radio receiver contemporaries, consists of an RF (Radio Frequency), IF (Intermediate Frequency) and Baseband section. In order to convert an intermediate signal to baseband signal, a series of filter and decimators are used. In embedded design power consumption is an important constraint. Design of decimation filter has more impact

on the power consumption at the receiver. The existing architecture of the 4G baseband receiver consumes more area and power, thus a necessity to increase area and power efficiency arises. So, this paper aims to develop an architecture that can be efficient in terms of power and area of a filter-decimator unit.

II. EXISTING METHODOLOGY

In 4G transmitter and receiver model the message signal of 100KHZ frequency, which decimated with a factor of 4. The transmitted signal at the receiver side contains the original message signal and the noise. The filter and decimator model at receiver retrieves the original signal.

Filter decimator model converts the IF signal to baseband signal, at receiver end. The received IF signal is mixed with an IF signal of same frequency, generated by Numerically Controlled Oscillator (NCO) and further multiplied with digital multiplier architecture, for IF signal to BB signal. The NCO architecture is implemented by Look up table based approach. The look up table stores the Sine/cosine values generated apriority utilizing the Taylor series. The multiplier architectures, commonly used Booth or Modified Booth architectures.

Then the signal is mixed and converted to a baseband signal according to the sampling frequency, after that filtering and decimation by a factor of 4 is performed. Fig 2 show the same design is implemented using FIR filter and series of decimating filter.
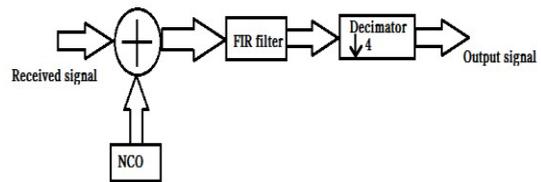

Fig 1.   The filter decimator architecture

NCO converts IF signal to BB signal. The filter specifications are Root Raised Cosine low pass filter which use rectangular window in the order of 64. The cut-off frequency of the filter is 15.36MHZ. Filter performs convolution operation; its output is given by

$$y(n) = x(n) * h(n) \ldots \ldots \ldots \ldots \ldots \ldots (1)$$

$$y(n) = \sum_{k=0}^{n} x(k)h(n-k) \ldots \ldots \ldots \ldots (2)$$

Decimator operation equation given by

$$y_n[n] = y[nM] \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots \ldots (3)$$

The receiver architecture consists of D flip flop, multiplier and adders. D flip flop acts as a memory which stores the input signal from the transmitter. The filter coefficient generated using MATLAB FDATOOL is given to the D flip flop. Then the stored coefficient multiplied with the impulse signal Figure.3. All signals from the multiplier is added and given to the decimator.
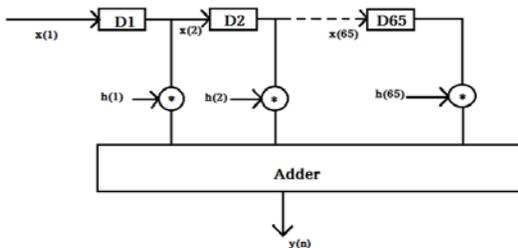

Fig 2.   FIR Filter architecture

The decimator down converts the signal by the factor of 4. The decimator reduces the anti-imaging at the receiver. In this method 13000 full adders where used. This increases the power and area of architecture of the 4G baseband receiver.

III. PROPOSED METHOD

The proposed architecture of the filter decimator model is shown in the figure.4. In this method the decimator is split into two factors. The FIR filter placed between two decimators by the factor of 2.

The received signal having sampling frequency 15.36MHz is given to the decimator then the decimated signal is given to the FIR filter which filters the decimated frequency by the sampling frequency 7.68MHz. As said before the power is directionally proportional to the frequency. The filter work at low frequency so the power used reduced by half. Then the signal given is decimated by the factor of 2. Instead of using FIR filter here the folded FIR filter is used, as the filter coefficients are symmetric. So in this method the number of 65 D flip flop is reduced to 33. The number of full adder used also reduced.
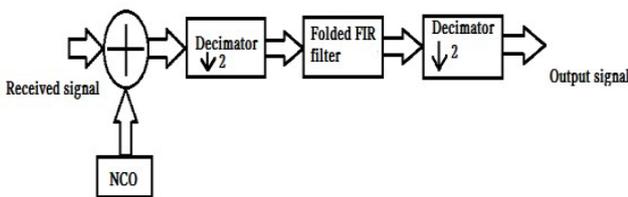

Fig 3.   Folded Filter Decimator Design

IV. RESULTS

The RRC filter coefficients are generated by MATLAB. Those coefficients are fed as an input to the filter architecture. The frequency response of the existing

method and proposed method are found out using MATLAB. The filter decimator architecture simulated using Modelsim.
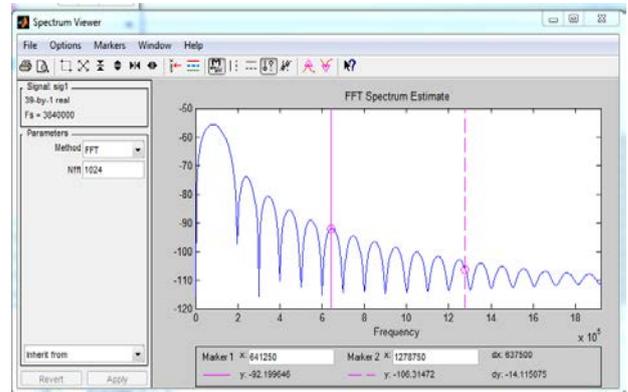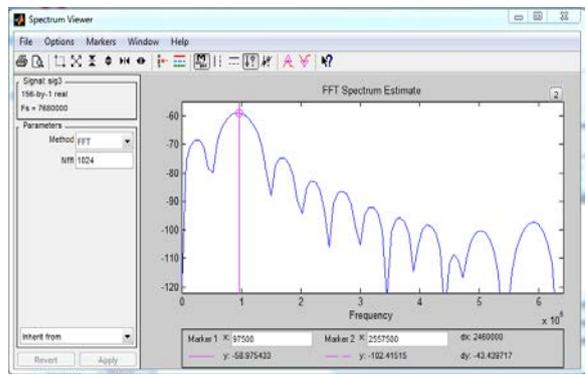

Fig 4.   Frequency response of existing method

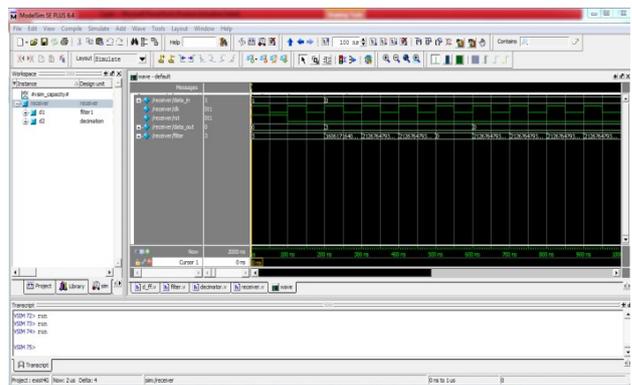Fig 5.   Frequency response of the proposed method

Fig 6.   Existing filter decimator architecture

V. CONCLUSION AND FUTURE WORK

In this paper the filter and decimator model for 4G baseband receiver was designed and simulated using MATLAB and Modelsim. The power and the area were reducing half in the proposed design. The future work will be the implementation of the architecture using FPGA to show the accurate difference between the two architecture models.

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